Applicants respectfully traverse the outstanding grounds for rejection, because in Applicants view the Stolmeijer et al patent clearly does not teach or obviate the claimed subject matter.

In particular, the semiconductor device recited in each of Claims 1, 7 and 13 is featured in that a base portion of a well area includes a low resistance area having a lower resistance value than that of the well area. As shown in Applicants' Figure 1 disclosure, for example, the recited low resistance area is the area 16, i.e., the base or bottom portion of the well area 13. As discussed hereinafter in more detail, it is respectfully submitted that the applied Stolmeijer et al. reference includes no such structure, and on the contrary shows the base regions of the well areas 120,130 to be of uniform resistance. Certainly, Stolmeijer et al. fail to teach a low resistance area not in contact with a depletion layer (e.g., DL of Figure 1) of a junction portion between the semiconductor layer (e.g., 15 of Figure 1) and the well area (e.g., 13 of Figure 1).

In contrast, Fig. 5 of Stolmeijer et al. shows a latch-up CMOS device in which p-well 130 and n-well 230 include field regions 120, 220, an isolation structure formed by trenches 71-75 filled with CVD oxide 50, and high doped regions 81-84 formed by implantation of p+ and n+ impurities in the top portions of the field regions 120, 220, respectively. Active devices 100 and 200 are formed in respective field regions 120, 220.

The outstanding Office Action in the "Response to Arguments" section states that Stolmeijer et al., column 3, lines 22-30 discloses that regions 120 and 220 of well regions 130 and 230 are heavily doped (less resistance). However, in fact, this portion of Stolmeijer et al., refers to the formation of "high dopant regions 81-84." Indeed, column 3, lines 22-30 of Stolmeijer et al. merely discloses that p+ impurities are introduced into field region 120 of p-well region 130, and n+ impurities are introduced into field region 220 of n-well region 230

to produce the high dopant regions 81-84. In addition, referring to Fig. 5 of Stolmeijer et al., "P+" and "N+" are added to high dopant regions 81-84, but not to regions 120 and 220.

In general, the impurity concentration of the field region of the well region is lower than those of the active region (110, 210) and the diffusion layer in the well region. When the impurity concentration is low, the resistance value is high.

Field regions 120 and 220 of Stolmeijer et al. are located under active regions 110 and 210. Thus, unless setting of the device of Stolmeijer et al. is specific, the impurity concentrations of field regions 120 and 220 are lower than those of active regions 110 and 210.

Furthermore, Stolmeijer et al., at column 3, lines 59-67 discloses a method of introducing dopants into the field region, and forming high dopant (doped field) regions 81-84 on the surfaces of field regions 120 and 220. Column 3, lines 59-67, however, does not disclose the impurity concentrations of the base or bottom portions of field regions 120 and 220. That is, the impurity concentrations of field regions 120 and 220 in the base portions thereof are uniform, and are equivalent to those of well regions 130 and 230. It is therefore believed to be quite clear that Stolmeijer et al. discloses no structural element corresponding to the low resistance area in pending Claims 1, 7 and 13.

While the "Response to Arguments" alleges that the field region 220 of the well 230 corresponds to the claimed low resistance area, Stolmeijer et al. clearly does not disclose a base portion of the field region 220 different in resistance than an area adjacent the base portion, and undeniably does not disclose, as stated for example in Claim 3, the field region having a low resistance area not in contact with a depletion layer (e.g., DL of Figure 1) of a

junction portion between the semiconductor layer (e.g., 15 of Figure 1) and the well area (e.g., 13 of Figure 1).[1]

It is further noted that the object of Stolmeijer et al. is to minimize the "dishing" effect of the isolation region, and reduce the latch up susceptibility due to high dopant regions 81-84. Therefore, Stolmeijer et al. does not disclose or suggest the structural features of Claims 1, 7, 13 and 16 or the advantages obtained thereby, as next discussed in more detail.

Stolmeijer et al. does not disclose the electrode of the capacitor in Claim 1 of the present application. According to claim 1, a low resistance area is provided at a base portion of a well area. Due to this structure, the resistance of the well can be kept low, even when the distance between the wiring lines connected to the electrode of the capacitor is increased to reduce the capacity of the wiring lines. Thus, the thermal noise can be suppressed. This advantage is not suggested in Stolmeijer et al.

According to claims 7 and 13, a low resistance area is provided at a base portion of a well area in which a MOSFET is formed. This structure can reduce the parasitic resistance of the well. Thus, the power loss can be reduced, and a high gain amplifier can be formed due to provision of the MOSFET. These advantages cannot be suggested in Stolmeijer et al.

According to claim 16, in a semiconductor device containing both an analog circuit and a digital circuit, a low resistance area is provided in a base portion of a first well area in

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[1] From paragraph 2 of the Office Action, it is appears that the Examiner considers the Stolmeijer et al. field region 220 of well region 230 as corresponding to the claimed "low resistance region." However, Stolmeijer et al. does not suggest that portions of the field region 220 have different resistances, and does not suggest that the base portion of the field region 220 is lower in resistance than a remainder of the field region 220, as a result of which it is not entirely clear how the Stolmeijer et al. reference is being construed by the Examiner. While Applicants consider that the claimed structure is clearly not disclosed by Stolmeijer et al., perhaps the rejection is based on a different interpretation of the claim language, and if that is the case, the Examiner is invited to telephone the undersigned to discuss claim changes which would harmonize the different interpretations.

which the analog circuit is provided. This structure prevents lowering of the gain of the analog circuit. This advantage is not suggested in Stolmeijer et al.

As is therefore believed to be clear from the above, claims 1-19 are not anticipated by or rendered obvious over Stolmeijer et al. Withdrawal of the outstanding grounds for rejection is therefore believed to be in order and is respectfully requested.

Consequently, in view of the present amendment and in light of the above comments, the pending claims are believed to be in condition for allowance, and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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